

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

**ECE2046 – COMPUTER ORGANIZATION AND
ARCHITECTURE**
(TE/EE/CE/OPE/NANO)

2 MARCH 2020
2:30 p.m – 4:30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 7 pages including cover page with 5 Questions only.
2. Attempt **ALL** Questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1 (25 marks)

- (a) The creation of this device / component revolutionizes computers. It was invented at Bell Labs in 1948 and commercialised in the late 1950s. It signals the beginning of the 2nd generation of computers. Name this device and list its advantages over the device it replaced.

[4 marks]

- (b) List the FOUR (4) main structural components of a general-purpose computer and briefly explain their functions.

[6 marks]

- (c) A set associative cache consists of 64 lines divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

[9 marks]

- (d) Draw a diagram and explain the fetch-execute cycle of a computer.

[6 marks]

Continued...

Question 2 (17 marks)

- (a) List down FIVE (5) operating system services provided to user.

[5 marks]

- (b) Explain the differences between uni-programming and multiprogramming.

[2 marks]

- (c) Describe the function of the “Resident Monitor Program” in main memory. Subsequently, draw the memory layout for Resident Monitor Program.

[4 marks]

- (d) With the aid of a diagram, discuss the five-states-process model involved in short-term scheduling.

[6 marks]

Continued...

Question 3 (17 marks)

- (a) Explain how to determine if a number is negative in the following representations: sign magnitude, two's complement, biased.

[2 marks]

- (b) Briefly describe the *Booth algorithm*. Use Booth algorithm to calculate the multiplication of $(-6_{10} \times 5_{10})$, and then verify the product obtained.

[Hint: Use 4-bit two's complement representation for both multiplicand and multiplier]

[8 marks]

- (c) Store the fractional number (199.125_{10}) using IEEE single precision floating-point format.

[3 marks]

- (d) Decode the following IEEE single precision floating-point number to its decimal equivalent:

1100 0100 1111 1100 1000 1000 0000 0000₂

[4 marks]

Continued...

Question 4 (25 marks)

- (a) Given the initial values (in decimal) in the accumulators with assembly code as follow:

P = 9, Q = 7, R = 6, S = 4, T = 2

Instruction 1 (I1): MOV X, P

Instruction 2 (I2): ADD X, Q

Instruction 3 (I3): MOV Y, R

Instruction 4 (I4): SUB Y, T

Instruction 5 (I5): MUL Y, S

Instruction 6 (I6): DIV Y, X

- (i) Determine the number of addresses of I5. [1 mark]
 - (ii) State TWO (2) characteristics of the addresses in I6. [2 marks]
 - (iii) Determine the value of accumulator X (in decimal) after I2 and before I3. [1 mark]
 - (iv) Determine the value of accumulator Y (in decimal) after I4 and before I5. [1 mark]
 - (v) Determine the value of accumulator Y (in decimal) after I6. [1 mark]
- (b) An address field in an instruction contains value **150**. Identify the location for corresponding operand for the following address modes:
- (i) Immediate Addressing. [1 mark]
 - (ii) Direct Addressing. [1 mark]
 - (iii) Indirect Addressing. [2 marks]

Continued...

- (c) In a control unit, the instructions have to be broken down further into micro-operations.
- (i) Describe the term micro-operations. [3 marks]
 - (ii) Discuss the different usage of the four internal registers of a microprocessor: Memory Address Register (MAR), Memory Buffer Register (MBR), Program Counter (PC), and Instruction Register (IR). [6 marks]
 - (iii) Write the possible sequence of micro-operations for the opcode **MUL R1, X**. [6 marks]

Continued...

Question 5 (16 marks)

- (a) Briefly explain the difference between pipelining and superpipelining architectures. [2 marks]
- (b) There are two superscalar architectures, namely Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC). Which of the two of these superscalar architectures is more complicated to implement? Justify your answer. [4 marks]
- (c) State FOUR (4) fundamental limitations of superscalar architecture. [4 marks]
- (d) The following programme instructions are referred:

Instruction 1: $R3 = R1 + R2$

Instruction 2: $R4 = R3 + 2$

Instruction 3: $R3 = R5 + 3$

- (i) Which TWO (2) instructions have output dependency? [2 marks]
- (ii) Give a reason for your answer in Q5d(i). [1 mark]
- (iii) Name the method that is used to solve output dependency and subsequently explain how this method works. [3 marks]

End of Paper

